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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,391	01/23/2004	Melany Ann Richmond	ZIL-555	8983

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,391	RICHMOND ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *23 January 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on January 23, 2004 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 19 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno).

As to claim 19, Bongiorno discloses a microcontroller integrated circuit (100) operable with an external first clock circuit (10), the microcontroller integrated circuit comprising: (a) a processor (80) having a system clock input lead (column 4, lines 2-8); (b) a terminal (switching circuit 66 within 60) for receiving a first clock signal generated by the external first clock circuit (column 4, line 61 thru column 5, line7); (c) a second clock circuit (20); and (d) means for detecting (timer 70) whether the first clock signal (10) is inadequate (malfunctioning) and, upon detecting that the first clock signal is inadequate, for decoupling (deselecting via switching means 66 within 60) the terminal from the system clock input lead and coupling (selecting via

switching means 66 within 60) the second clock circuit (20) to the system clock input lead, wherein the means decouples (deselects) the terminal from the system clock input lead and couples the second clock circuit (20) to the system clock input lead without receiving any signal from the processor (Bongiorno discloses a clock selection circuit wherein a timer [70] that can be a separate circuit from the microprocessor [80] and detects a first clock circuit [10] is inadequate [malfunctioning], deselects the first clock [10] via switching means [66 within 60] and selects and second clock circuit [20] also using the switching means; column 4, lines 9-34 and column 4, line 61 thru column 5, line 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno) in view of Kim (U.S. Patent No. 6,845,454 B2) (hereinafter referred to as Kim).

As to claim 1, Bongiorno discloses a method comprising: (a) detecting (via timer 70) whether a first clock signal (from clock source 10) is inadequate, wherein the first clock signal is generated by a first clock circuit (Bongiorno discloses a clock detecting and selecting method wherein a first clock signal from a first clock circuit [10] is detected to be inadequate [malfunctioning] via timer [70] column 4, lines 2-21 and column 4, lines 41-43); (b) decoupling

(deselecting) the first clock circuit (10) from a system clock input lead of a processor (Bongiorno discloses the inadequate [malfunctioning] clock circuit [10] being deselected [via switching means 66 within 60] from a processor [80]; column 4, line 61 thru column 5,line 7); (c) coupling (selecting) a second clock circuit (20) to the system clock input lead of the processor (Bongiorno discloses a second clock circuit [20] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7); (e) decoupling (deselecting) the second clock circuit (20) from the system clock input lead of the processor (Bongiorno discloses the inadequate [malfunctioning] clock circuit [20] being deselected [via switching means 66 within 60] from a processor [80]; column 4, line 61 thru column 5,line 7); and (f) coupling (selecting) a third clock circuit (30) to the system clock input lead of the processor (Bongiorno discloses a third clock circuit [30] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7).

Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit.

Kim teaches a processor clock generation circuit (100) wherein a clock circuit (110) can be enabled (powered on/off) by selecting the clock circuit (110) via clock selector (140) and clock controller (130) wherein power is applied to a switch (115) within the clock circuit (110) to enable (power on) the clock circuit (column 2, line 66 thru column 3, line 20). Kim also has the additional feature of placing the processor into sleep mode by selecting a slower clock and powering down the fast clock that is no longer needed (column 2, lines 41-56).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kim at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to power off unnecessary clock circuits as taught by Kim such that when selecting a clock to use the clock circuit is enabled/powered on first then coupled and the failing/unnecessary clock in disabled/powered off. One of ordinary skill in the art would be motivated to make this combination of enabling/powering on necessary clock circuits and disabling/powering on selected clock circuits in view of the teachings of Kim, as doing so would give the added benefit of selecting slower clock circuits to place a processor into a sleep mode (column 2, lines 41-56).

As to claim 2, Bongiorno discloses the method wherein the first clock circuit a high-speed, external crystal oscillator, wherein the second clock circuit is a low-speed, internal watchdog timer, and wherein the third clock circuit is a high-speed, internal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-25).

As to claim 3, Bongiorno discloses the method wherein the detecting is performed by detecting no signal edges of the first clock signal during a time period over which a linear feedback shift register increments to a predetermined value (Bongiorno discloses the timer monitoring the processor clock signal such that a predetermined count value [pre-set time-out

period] is incremented, as is known in the art, which can be done with or without an LFSR; column 1, lines 26-39).

As to claim 4, Bongiorno discloses the method wherein the decoupling the first clock circuit in (b) is not performed as a result of a signal from the processor (Bongiorno discloses the decoupling [deselecting] is carried out as a result from the watchdog timer [70] which may or may not be part of the microprocessor; column 4, lines 9-21).

As to claim 5, Bongiorno discloses the method wherein the coupling the second clock circuit in (c) is not performed as a result of a signal from the processor (Bongiorno discloses the coupling [selecting] is carried out as a result from the watchdog timer [70] which may or may not be part of the microprocessor; column 4, lines 9-21).

As to claim 6, Kim teaches the method wherein the third clock circuit is enabled in (d) by powering up the third clock circuit (column 3, lines 8-20).

As to claim 7, Bongiorno discloses the method further comprising, between step (a) and step (b): sending an interrupt signal (reset signal) to the processor indicating that the first clock circuit has failed (column 4, lines 9-21).

As to claim 8, Kim teaches the method further comprising, between step (a) and step (b): (g) disabling a failure detection circuit that performed the detecting in (a) (Kim teaches the detection circuit of the clock selection circuit receives a "sleep" command from the processor itself which is the device detecting the sent interrupts and sleep commands to turn the unwanted, fast clock off; column 3, lines 26-34).

As to claim 9, Bongiorno discloses the method further comprising, between step (d) and step (e): (g) detecting (via detector 50) whether a second clock signal is inadequate, wherein the

second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 10, Kim teaches the method wherein the first clock circuit can be coupled to the system clock input lead by a multiplexer (160), the first clock circuit being coupled to a first data input lead of the multiplexer, wherein the second clock circuit is coupled in (c) to the system clock input lead by the multiplexer, the second clock circuit being coupled to a second data input lead of the multiplexer, wherein a third data input lead of the multiplexer is grounded, and wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead (Kim teaches the clock selection circuit comprising a multiplexer [160] to select the appropriate clock signal to be sent to the processor such that the combination of Bongiorno in view of Kim can provide a three-input multiplexer to select any of the three desired clock signals; column 3, lines 52-56).

As to claim 11, Bongiorno discloses an integrated circuit, comprising: (a) a processor (80) with a system clock input lead (column 4, lines 2-8); (b) a terminal (switching circuit 66 within 60), the terminal coupled to a first clock circuit (10), the first clock circuit generating a first clock signal (column 4, line 61 thru column 5, line7); (c) a second clock circuit (20); (d) a third clock circuit (30); and (e) a clock controller (40) coupled to the system clock input lead (as shown in figure 1B; column 4, lines 2-8), wherein the clock controller is adapted to decouple (deselect via switching means 66 within 60; Bongiorno discloses the inadequate [malfunctioning] clock circuit [10] being deselected [via switching means 66 within 60] from a processor [80]; column 4, line 61 thru column 5,line 7) the system clock input lead from the terminal and to couple (select via switching means 66 within 60; Bongiorno discloses a second

clock circuit [20] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7) the system clock input lead to the second clock circuit (20) upon detecting that the first clock signal is inadequate (malfunctioning), and wherein the clock controller is further adapted to select the third clock circuit (30) upon detecting that the first clock signal is inadequate (Bongiorno discloses a third clock circuit [30] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7).

Bongiorno fails to disclose the clock controller is adapted to turn on the third clock circuit.

Kim teaches a processor clock generation circuit (100) wherein a clock circuit (110) can be enabled (powered on/off) by selecting the clock circuit (110) via clock selector (140) and clock controller (130) wherein power is applied to a switch (115) within the clock circuit (110) to enable (power on) the clock circuit (column 2, line 66 thru column 3, line 20). Kim also has the additional feature of placing the processor into sleep mode by selecting a slower clock and powering down the fast clock that is no longer needed (column 2, lines 41-56).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kim at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to power off unnecessary clock circuits as taught by Kim such that when selecting a clock to use the clock circuit is enabled/powered on first then coupled and the failing/unnecessary clock in disabled/powered off. One of ordinary skill in the art would be motivated to make this combination of enabling/powering on necessary clock circuits and

disabling/powering on selected clock circuits in view of the teachings of Kim, as doing so would give the added benefit of selecting slower clock circuits to place a processor into a sleep mode (column 2, lines 41-56).

As to claim 12, Bongiorno discloses the integrated circuit wherein the first clock circuit is a high-speed external crystal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-25).

As to claim 13, Bongiorno discloses the integrated circuit wherein the second clock circuit is a low-speed, internal watchdog timer (column 4, lines 9-15) oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-25).

As to claim 14, Bongiorno discloses the integrated circuit wherein the clock controller can decouple the system clock input lead from the terminal when the processor is receiving an inadequate first clock signal (Bongiorno discloses the decoupling [deselecting] is carried out as a result from the watchdog timer [70] which may or may not be part of the microprocessor; column 4, lines 9-21).

As to claim 15, Bongiorno discloses the integrated circuit wherein the clock controller decouples the system clock input lead from the second clock circuit and couples the system clock input lead to the third clock circuit (Bongiorno discloses the coupling [selecting] and decoupling [deselecting] is carried out as a result from the watchdog timer [70] which may or may not be part of the microprocessor; column 4, lines 9-21).

As to claim 16, Bongiorno discloses the integrated circuit wherein the clock controller comprises a primary clock source fail detect circuit (timer 70), and wherein the primary clock source fail detect circuit detects whether the first clock signal inadequate (column 4, lines 9-21).

As to claim 17, Bongiorno discloses the integrated circuit wherein the clock controller further comprises a secondary clock source fail detect circuit, and wherein the secondary clock source fail detect circuit detects whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 18, Bongiorno discloses the integrated circuit wherein the clock controller comprises a plurality of substantially identical clock source fail detect circuits, and wherein each of the clock source detect circuits detects whether a different clock signal is inadequate (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno) as applied to claim 19 above, and further in view of Kim (U.S. Patent No. 6,845,454 B2) (hereinafter referred to as Kim).

As to claim 20, Bongiorno discloses the microcontroller integrated circuit further comprising: (e) a third clock circuit (30), wherein the means (switching means 66 within 60) selects the third clock circuit upon detecting that the first clock signal is inadequate (column 4, lines 9-34). However, Bongiorno fails to disclose the third clock circuit being turned on.

Kim teaches a processor clock generation circuit (100) wherein a clock circuit (110) can be enabled (powered on/off) by selecting the clock circuit (110) via clock selector (140) and clock controller (130) wherein power is applied to a switch (115) within the clock circuit (110) to enable (power on) the clock circuit (column 2, line 66 thru column 3, line 20). Kim also has the additional feature of placing the processor into sleep mode by selecting a slower clock and powering down the fast clock that is no longer needed (column 2, lines 41-56).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kim at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to power off unnecessary clock circuits as taught by Kim such that when selecting a clock to use the clock circuit is enabled/powered on first then coupled and the failing/unnecessary clock in disabled/powered off. One of ordinary skill in the art would be motivated to make this combination of enabling/powering on necessary clock circuits and disabling/powering on selected clock circuits in view of the teachings of Kim, as doing so would give the added benefit of selecting slower clock circuits to place a processor into a sleep mode (column 2, lines 41-56).

As to claim 21, Bongiorno disclose the microcontroller integrated circuit wherein the means decouples the second clock circuit from the system clock input lead and couples the third

clock circuit to the system clock input lead after the turning on of the third clock circuit (column 4, lines 22-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

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May 12, 2006

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